REMARKS/ARGUMENTS

Reconsideration and allowance of this application are respectfully requested in view of the following remarks.

Claims 12, 15-16, 18, 21 and 23 stand rejected under 35 USC §102(e) as being anticipated by Chen et al. (U.S. Patent No. 6,532,018). Claims 1, 3-8 and 10 stand rejected under 35 USC §103(a) as being obvious over Chen et al. ('018) in view of Migdal (U.S. Patent No. 6,426,753). Dependent claims 11, 13, 14, 17, 19, 20 and 22 stand rejected under 35 USC §103(a) as being obvious over Chen et al. in view of Migdal '753 and further in view of Nally (U.S. Patent No. 5,506,604) and, in addition, dependent claims 13, 14, 17, 19, 20 and 22 stand rejected under 35 USC §103(a) as being obvious over Chen et al. in view of Nally et al. '604 and further in view of Nakamura et al. (U.S. Patent No. 6,384,831). In addition, independent claim 24 stands rejected under §102(e) as being anticipated by Yasumoto (U.S. Patent 6,747,642).

By this amendment, claims 1, 3, 4, 10, 12-16, 18 and 23 are cancelled without prejudice or disclaimer. Claims 5-7, 11, 17, 19-22 and 24, as amended, and new claims 25 and 26 are now presented for consideration.

Applicants respectfully submit that newly presented independent claims 25 and 26, as well as claims dependent thereon, are not anticipated by or rendered obvious by the cited references or any prior art of record, for at least the following reasons:

The rejection of claims 12, 15-16, 18, 21 and 23 under 35 U. S. C. §102(e) as being anticipated by Chen et al. (U.S. Patent No. 6,532,018) is respectfully traversed. Claims 12-16, 18 and 23 are cancelled without prejudice or disclaimer and claims 19-22 are now dependent from newly presented independent claim 26.

Newly presented independent claim 26 recites a method of transferring data from an embedded frame buffer on a graphics processing chip in a graphics processing system to a separate main memory of the graphics processing system and, moreover, further requires: storing RGB format image data in the embedded frame buffer of the graphics processing chip; initiating a copy out operation for transferring image data from the embedded frame buffer to the main memory of the graphics system (which is an off-chip "external" storage destination); converting the image data from an RGB format to a YUV display format during a copy out operation between the embedded frame buffer and the graphics processing system's main memory (so as to reduce the total amount of storage space needed to store the image data in main memory which results in an increase in main memory bandwidth when displaying (reading out) image data from the main memory); and, writing the converted image data to a separate frame buffer located in the graphics processing system's main memory which is provided on a separate chip from the graphics processing chip. Applicants respectfully contend that the above combination of features are not disclosed by Chen et al. in the '018 patent.

Independent claim 26 recites storing image data in RGB format and converting the stored image data from an RGB format to a YUV display format during the copy out operation for writing the converted data to the separate non-embedded main memory of the graphics system. Applicants contend that Chen et al.'s suggestion of performing *some* formatting prior to displaying on a monitor (See Chen et al. patent at column 2, lines 42-46.) does not anticipate or even suggest Applicants' claimed process of converting pixel data from an RGB format to a YUV display format during the copy out

operation between an embedded frame buffer and a separate non-embedded main memory, as set forth in Applicants' claim 26.

Applicants also respectfully traverse the 09/17/05 Office Action contention that Chen et al. discloses Applicants' claimed feature of using a copy pipeline to transfer the data from an embedded frame buffer to an external memory. Applicants contend that the cited passages relied upon in the '098 Chen et al. patent at most disclose only *copying data to different locations within the same M chip*, and do not teach or disclose copying image data from an embedded frame buffer on a graphics processor chip *to a separate non-embedded main memory* of the graphics system, as set forth in Applicants' claim 26.

In addition, Applicants further contend that the '018 Chen et al. patent clearly teaches away from writing converted image data to a separate non-embedded main memory, as set forth in Applicants' claims, for at least the reason that Chen et al. is primarily concerned with reducing the latency that occurs when writing to an external off-chip memory. (See, for example, the Chen et al. '018 patent at column 2, lines 4-6 and lines 53-56, column 4, lines 48-50 and column 5, lines 2-4 wherein Chen et al. explicitly state that "[T]he data never needs to leave the substrate.")

For at least the reasons stated above, Applicants contend that the Chen et al. patent does not anticipate independent claim 26 or any of the claims dependent thereon because it does not disclose every element of the invention as claimed. See *Lewmar Marine, Inc. v. Barient, Inc.*, 3 U.S.P.Q. 2d 1766 (Fed. Cir. 1987).

The rejection of claims 1, 3-8 and 10 under 35 U.S.C. §103 as being unpatentable over Chen et al. ('018) in view of Migdal (U.S. Patent No. 6,426,753) and,

in addition, the rejection of dependent claims 11, 13, 14, 17, 19, 20 and 22 as being obvious over Chen et al. ('018) in view of Migdal ('753) and further in view of Nally et al. (U.S. Patent No. 5,506,604), is respectfully traversed. Independent claim 1 and dependent claims 3, 4, 8, 10, 13 and 14 are cancelled without prejudice or disclaimer. Dependent claims 5-7 and 11 are now dependent from new independent claim 25 and dependent claims 17 and 19-22 are now dependent from new independent claim 26.

Independent claim 25 recites a graphics system, comprising: a pixel data post-processing copy-out pipeline that selectively converts pixel data from one image format to another during a reading and transfer of the data from the embedded frame buffer to a separate non-embedded main memory of said graphics system, wherein the copy-out pipeline is operable to selectively transfer the data to either a display buffer area or a texture buffer area within said main memory and wherein the copy-out pipeline converts the data to a display format if the data is transferred to the display buffer area and converts the data to a texture format if the data is transferred to the texture buffer area. Applicants respectfully contend that the '018 Chen et al. reference fails to teach or suggest converting the image data to a display format if the data is transferred to a display buffer area and converting the image data to a texture format if the data is transferred to a texture buffer area, as set forth by independent claim 25. The '018 Chen et al. reference also fails to teach or suggest the above claimed features for at least the same reasons as set forth above with respect to independent claim 26.

Moreover, Applicants respectfully contend that the Migdal ('753) reference neither teaches nor suggests the above recited features of claim 25 either when considered alone or together with Chen et al. or any other reference of record. At the

outset, Migdal fails to teach or suggest any type of copy-out pipeline arrangement per se. Indeed, the Migdal '753 patent is directed toward a distributed frame buffer and texture cache memory arrangement implemented using a high bandwidth network. Applicants contend that there is no teaching or suggestion by either Chen et al. or Migdal of a copy-out pipeline arrangement for a graphics system in which pixel data is copied from a frame buffer memory instantiated on the same semiconductor chip as a graphics coprocessor to a separate non-embedded main memory as set forth in Applicants' claims. In fact, the very nature of Migdal's distributed memory arrangement clearly teaches away from Applicants' claimed arrangement *as there is no "main memory" per se* in Migdal's *distributed* memory arrangement and, moreover, there would be no need to copy-out data to such a separate main memory. When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references. See *In re Geiger*, 815 F. 2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987).

In addition, Applicants respectfully contend that there is no teaching by Migdal that would suggest the obviousness of modifying the system of Chen et al. to implement a copy-out pipeline or to provide a separate non-embedded main memory separate from Chen et al.'s combined logic and memory chip. Moreover, there is no teaching or suggestion by Migdal to selectively transfer data to either a display area buffer or a texture area buffer or to provide specific format conversions dependent upon whether the data is copied out to a display buffer area or a texture buffer area in main memory, as set forth in Applicants' claim 25. Applicants respectfully contend that the Office Action improperly relies on hindsight reconstruction of the claimed invention based on

the teachings of the instant application in reaching its obviousness determination. "To imbue one of ordinary skill in the art with knowledge of the invention, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." See *W.L. Gore & Assoc. v. Garlock, Inc.*, 721 F.2d 1540, 1543, 220 USPQ 303, 312-13 (Fed. Cir. 1983). Only in view of the teachings of the instant application could the rejections possibly be maintained.

Likewise, although directed toward processing video data from a first YUV format to a second YUV format, the Nally et al. ('604) patent fails to make up for the deficiencies of the Chen et al. and Migdal references as discussed above. Accordingly, it is submitted that independent claims 25 and 26 and claims 5-7, 11, 17 and 19-22 dependent thereon are patentably distinct over the combined teachings of Chen et al. ('018) in view of Migdal ('753) and/or further in view of Nally et al. ('604).

The rejection of dependent claims 13, 14, 17, 19, 20 and 22 as being obvious over Chen et al. in view of Nalley et al. and further in view of Nakamura et al. ('831) is also respectfully traversed. Nakamura et al. discloses, among other things, a graphic processor system capable of computing a weighted average of pieces of pixel data. However, Nakamura et al. fail to make up for the deficiencies of the Chen et al. and Nalley et al. references for at least the same reasons as set forth above with respect to independent claim 26.

The rejection of claim 24 under 35 U. S. C. §102(e) as being anticipated by Yasumoto (U.S. Patent 6,747,642) is respectfully traversed. Yasumoto suggests only that "pixel filter 50 may operate to apply border line cartoon outlining" but does not

disclose or suggest selecting a sub-region of pixels in the embedded frame buffer as a source for pixel data transfer or the performing of anti-aliasing or de-flickering as a part of the pixel post-processing. Consequently, Applicants respectfully contend that the Yasumoto patent does not anticipate independent claim 24 at least because it does not disclose every element of the invention as claimed. See *Lewmar Marine, Inc. v. Barient, Inc.*, 3 U.S.P.Q. 2d 1766 (Fed. Cir. 1987).

Having fully responded to all of the pending objections and rejections contained in this Office Action, Applicants submit that all claims now remaining in the present application are in condition for allowance and earnestly solicit an early Notice to that effect. The Examiner is invited to contact the undersigned if any further information is required.

Respectfully submitted,

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